Amendments to the claims:

Please cancel claims 3 and 11, amend claims 1 and 9, and add new claims 21 and 22 as shown in the following listing of claims. This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (currently amended) An integrated circuit comprising:

a substrate; and

a high electron mobility transistor formed on the substrate, the high electron mobility transistor including a source electrode, a drain electrode and a gate electrode, the high electron mobility transistor having an increased gate-to-drain etch recess spacing, wherein the increased gate-to-drain etch recess spacing is at least four microns, the increased gate-to-drain etch recess spacing proving a greater protection for the high electron mobility transistor from an electrostatic discharge on the drain electrode.

2. (original) The integrated circuit of claim 1 wherein the high electron mobility transistor includes an enhancement mode pseudomorphic high electron mobility transistor.

3. (canceled).

4. (original) The integrated circuit of claim 1 further comprising a second high electron mobility transistor formed on the substrate on a signal path between an input node and an output node, the second high electron mobility transistor having a second gate-to-drain etch recess spacing, the gate-to-drain etch recess spacing of the high electron mobility transistor being wider than the second gate-to-drain etch recess spacing of the second high electron mobility transistor.

5. (original) The integrated circuit of claim 4 wherein a width of the gate electrode of the high electron mobility transistor is wider than a width of a gate electrode of the second high electron mobility transistor.

6. (original) The integrated circuit of claim 1 further comprising a resistor formed over the substrate connected to the drain electrode of the high electron mobility transistor, the resistor being made of a semiconductor material.

7. (original) The integrated circuit of claim 1 further comprising a reverse biased Schottky diode formed over the substrate connected to the drain electrode of the high electron mobility transistor, the reverse biased Schottky diode being configured to have an increased anode-to-cathode etch recess spacing to provide protection for the reverse biased Schottky diode from a positive electrostatic discharge.

8. (original) The integrated circuit of claim 7 wherein the reverse biased Schottky diode is structurally configured to turn on prior to the high electron mobility transistor when a negative electrostatic discharge is applied to the drain electrode of the high electron mobility transistor.

9. (currently amended) A method for fabricating an integrated circuit with at least one high electron mobility transistor, the method comprising:

proving a substrate; and

forming a high electron mobility transistor with a source electrode, a drain electrode and a gate electrode on the substrate, including creating an increased gate-to-drain etch recess spacing of at least four microns, the increased gate-to-drain etch recess spacing proving a greater protection for the high electron mobility transistor from an electrostatic discharge on the drain electrode.

10. (original) The method of claim 9 wherein the forming of the high electron mobility transistor includes forming an enhancement mode pseudomorphic high electron mobility transistor on the substrate.

11. (canceled).

12. (original) The method of claim 9 further comprising forming a second high electron mobility transistor on the substrate on a signal path between an input node and an output node, the second high electron mobility transistor having a second gate-to-drain etch recess spacing, the gate-to-drain etch recess spacing of the high electron mobility transistor being wider than the second gate-to-drain etch recess spacing of the second high electron mobility transistor.

13. (original) The method of claim 12 wherein the forming the high electron mobility transistor includes creating the gate electrode with a width that is wider than a width of a gate electrode of the second high electron mobility transistor.

14. (original) The method of claim 9 further comprising forming a resistor over the substrate connected to the drain electrode of the high electron mobility transistor, the resistor being made of a semiconductor material.

15. (original) The method of claim 9 further comprising forming a reverse biased Schottky diode over the substrate connected to the drain electrode of the high electron mobility transistor, including creating an increased anode-to-cathode etch recess spacing to provide protection for the reverse biased Schottky diode from a positive electrostatic discharge.

16. (original) An integrated circuit comprising:

an insulating substrate;

a first high electron mobility transistor formed on the insulating substrate, the first high electron mobility transistor having a first gate-to-drain etch recess spacing; and

a second high electron mobility transistor formed on the insulating substrate, the second high electron mobility transistor having a second gate-to-drain etch recess spacing that is wider than the first gate-to-drain etch recess spacing of the first high electron mobility transistor to provide a greater protection for the second high electron mobility transistor from an electrostatic discharge.

17. (original) The integrated circuit of claim 16 wherein the second gate-to-drain etch recess spacing of the second high electron mobility transistor is at least four microns.

18. (original) The integrated circuit of claim 16 wherein a width of a gate electrode of the second high electron mobility transistor is wider than a width of a gate electrode of the first high electron mobility transistor.

19. (original) The integrated circuit of claim 16 further comprising a resistor formed over the substrate connected to a drain electrode of the second high electron mobility transistor, the resistor being made of a semiconductor material.

20. (original) The integrated circuit of claim 16 further comprising a reverse biased Schottky diode formed over the insulating substrate connected to the second high electron mobility transistor, the reverse biased Schottky diode being configured to have an anode-to-cathode etch recess spacing that is wider than the first gate-to-drain etch recess spacing of the first high electron mobility transistor to provide protection for the reverse biased Schottky diode from the positive electrostatic discharge.

21. (new) A method for fabricating an integrated circuit with at least one high electron mobility transistor, the method comprising:

proving a substrate;

forming a high electron mobility transistor with a source electrode, a drain electrode and a gate electrode on the substrate, including creating an increased gate-to-drain etch recess spacing, the increased gate-to-drain etch recess spacing proving a greater protection for the high electron mobility transistor from an electrostatic discharge on the drain electrode; and

forming a second high electron mobility transistor on the substrate on a signal path between an input node and an output node, the second high electron mobility transistor having a second gate-to-drain etch recess spacing, the gate-to-drain etch recess spacing of the high electron mobility transistor being wider than the second gate-to-drain etch recess spacing of the second high electron mobility transistor.

22. (new) The method of claim 21 wherein the forming the high electron mobility transistor includes creating the gate electrode with a width that is wider than a width of a gate electrode of the second high electron mobility transistor.